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Power Factor Correction in Distribution System Using DSTATCOM with the Help of MATLAB Simulink

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Abstract— — In this paper, an implementation of three phase synchronous reference frame (SRF) theory based control algorithm for functions of DSTATCOM in power factor correction (PFC) under nonlinear distribution system. A SRF theory based control algorithm is used for extraction of fundamental active and reactive power components of load currents. These components are used for estimation of reference source currents. The DSTATCOM is developed in three phase system and its real time performance is studied using MATLAB Simulink. The performance of DSTATCOM is found satisfactory with proposed control algorithm for nonlinear distribution system.

Index Terms— — SRF Theory, DSTATCOM, Power Factor Correction, MATLAB Simulink, VSC, Reactive Power Compensation, Non Linear Load. SRF Theory, DSTATCOM, Power Factor Correction, MATLAB Simulink, VSC, Reactive Power Compensation, Non Linear Load.

1 INTRODUCTION

The power quality problem in AC distribution system are mainly proliferation of different type of nonlinear loads, unplanned expansion of distribution system etc. These power quality problems include high reactive power burden, harmonic currents, load unbalance and excessive neutral currunt [1-6]. The power qualti at point of common coupling (PCC) is regulated by various standards such as IEEE-519 standard [7]. Three phase DSTATCOM is used for voltage regulation or power facor improvement, harmonic elimination and load balancing in three-phase system with linear and nonlinear load [8-9]. The performance of DSTATCOM is depands upon the selection of control algorithm and design. There are different type of algorithms are present for extracts the reference source currents to control the DSTATCOM such as Instantaneous Reactive Power (IRP) theory, Instantaneous Symmetrical Componanets (ISC), PI controller based algorithms, Current Synchronous Detection (CSD), p-q theory based control algorithm are present in literature [10-12].

In this paper, a DSTATCOM is implemented with three phase distribution system, which is based on synchronous reference (SRF) theory for extraction of load current [13]. This control algorithm on DSTATCOM is implemented for harmonic compensation, power factor correction and current compensation at source in distribution level with nonlinear loads. The three-leg VSC compensates the harmonic current and reactive power and balances the load. The insulated gate bipolar transistor (IGBT) based VSC is self-supported with a dc bus capacitor and is controlled for the required compensation of load current. The DSTATCOM is designed and simulated using MATLAB software with its Simulink and power system block set (PSB).

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2 SYSTEM CONFIGRATION

Fig. 1 shows the single line diagram of the shunt-connected DSTATCOM based distribution system. The dc capacitor connected at the dc bus of converter acts as an energy buffer and stablishhes a dc voltage for normal operaion of DSTATCOM system. The DSTATCOM can be operated for reactive power compensation for power factor correction. The DSTATCOM injects a current I_c such that the source current is only i_c and this is in-phase with voltage.

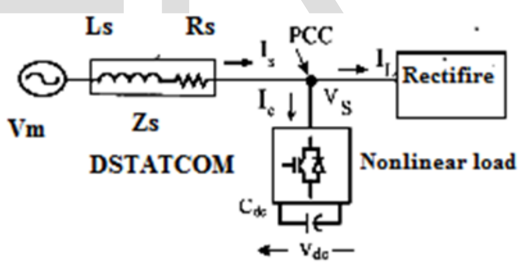

Fig. 1 Single line diagram of DSTATCOM

Fig. 2 shows schematic diagram of DSTATCOM using three phase VSC with improved power quality at existing distribution system. A diode rectifier with R-L load is modelled as nonlinear load which characteristics are common is the distribution system. A passive ripple filter is connected at PCC for filtering the high frequency switching noise due to switching of VSC from AC mains. Symbol L_s and R_s are presented as grid source impedance. For a considered nonlinear load, the design data DSTATCOM is given in Appendix. The DSTATCOM has six IGBTs, three ac inductors and one dc capacitor. The required compensation to be provided by the DSTATCOM desides the rating of the VSC componenets. The data of DSTATCOM system considered for analysis is shown in the Appendix. The selection of interfacing inductor, dc capacitor and the ripple filter are given in folling section:

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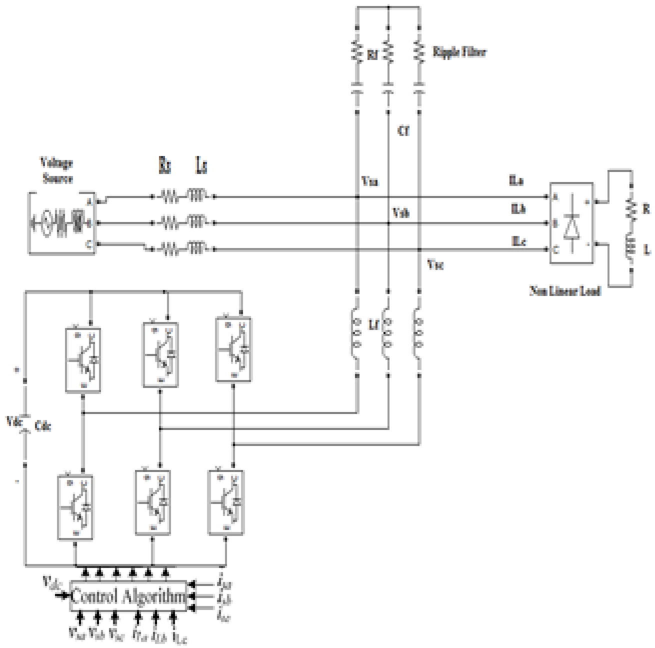

Fig. 2 Schematic diagram VSC based DSATCOM

2.1 DC Capacitor Voltage

The minimum dc bus voltage of VSC of DSATCOM should be greater than twice the peak of phase voltage of system. The dc bus voltage is calculated as

$$Vdc = \frac{2\sqrt{2}Vll}{\sqrt{3}m}$$

Where m is the modulation index and is considered index as 1 and V_{ll} is the ac line output voltage of DSTATCOM. Thus V_{dc} is obtained as 677.69 for V_{ll} of 415 and is selected as 700 V.

2.2 DC Bus Capacitor

The value of dc capacitor (C_{dc}) of VSC of DSATCOM depannds upon inatantaneous energy available to the DSATCOM during transients. The principle of energy conservation is applied as

$$\frac{1}{2}Cdc[(Vdc^2) - (Vdc1^2)] = 3V(aI)t$$

Where V_{dc} is reference dc voltage and V_{dc1} is minimum voltage level of dc bus, a is overloading factor, V is phase voltage, I is phase current and t is time by which the dc voltage is to recovered. Considering the minimum voltage level of dc bus bus V_{dc1}= 690, V_{dc} = 700 V, V= 239.60 V, I = 27.82 A, t 350 micro seconds, a= 1.2. The calculated value of C_{dc} is 2600 micro Farad and selected as 3500 micro Farad.

2.3 AC Inductor

The selection of the ac inductance (L_f) of VSC depands upon currents ripple $i_{cr\ p\text{-}p}$, switching frequmcy f_s dc bus voltage (V_{dc}). AC inducatance is mainly these parameters and is calculated by using these parameters. The formula for calculation of AC inducatance is given as

$$Lf = \frac{\sqrt{3}mVdc}{12afs\ icr(p-p)}$$

Where m is the modulation index and overloading factor. Consider $i_{cr\ p\text{-}p}$= 5%, f_s = 10 kHz, m= 1, Vdc = 700 V, a=1.2, the L_f value is calculated to be 2.44 mH. A round-off value of L_f of 2.5 mH is selected in this investigation.

2.4 Ripple Filter

A low-pass first-order filter tuned at half the swiching frequency is used to filter the high-frequency noise from the voltage at PCC. Considering a low impedance of 8.1 oham, for harmonic voltage at the frequency of 5 kHz, the ripple filter capacitor is designed as C_f = 10 micro farad. A series resistance (R_f) of the 5 ohms is included in series with the capacitor (C_f). The impedance of fundamental frequency, which is sufficiently large, and hence the ripple filter draws negligible fundamenatal current.

3 CONTROL ALGORITHM

The control approach used for estimation of reference AC mains currents for the control of VSC is a synchronous reference frame theory (SRFT). The SRF theory based on the transformation of load currents in synchrounous rotating d-q frame. This control system is shown in fig.3.

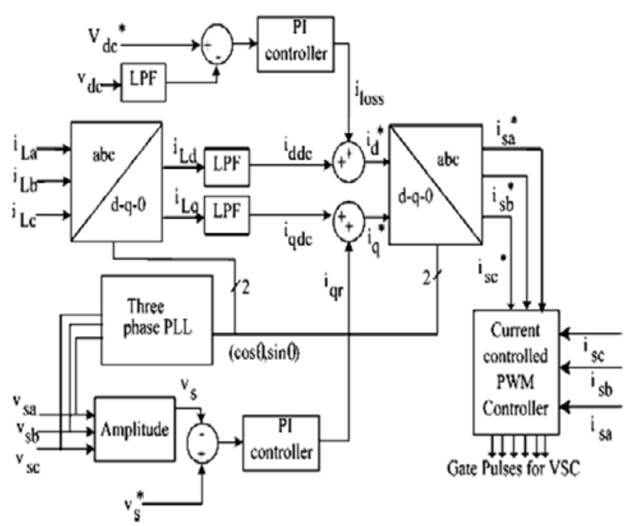

Fig. 1 Generation of reference currents using SRF theory based control algorithm

Load currents (i_{la}, i_{lb}, i_{lc}), (PCC) voltages (V_{sa}, V_{sb}, V_{sc}) and DC bus voltage (V_{dc}) of VSC are sensed as feedback signals. Load currents forms abc frame are converted to dq0 frame using folling transformation:-

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$$\begin{bmatrix} iLq \\ iLd \\ iL0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} iLa \\ iLb \\ iLc \end{bmatrix}$$

Where cos Φand sinΦ are obtained using a three-phase locked loop (PLL). A PLL signal is obtained from terminal voltages for generation of fundamental unit vectors for conversion of sensed currunts to the d-q-0 referance frame. The SRF controller extracts dc quantities by low pass filter, and hence the non dc quantities (hormonics) are separated from the reference signal. The d-axix and q-axis currents consist of fundamental and harmonic componenet as

$$I_{Ld} = i_{d\,dc} + i_{d\,ac}$$
$$I_{Lq} = i_{q\,dc} + i_{q\,ac}$$

The control strategy for reactive power compensation for UPF operation considers that the source must deliver the mean value of the direct-axis component of the load current along with the active power component current for maintain the dc bus and meeting losses ($I_{loss)}$ in DSATCOM. The output of proportional-integral (PI) controller at the dc bus voltage of DSATCOM is considerd as the current (I_{loss}) for meeting its losses;

$$I_{loss}(n) = I_{loss}(n\text{-}1)+K_{pd}\{V_{de}(n)\text{-}V_{de}(n\text{-}1)+K_{id}V_{de}(n)$$

Where $V_{de}(n) = V_{dc}^{*}$- $V_{dc}(n)$ is error between the reference V_{dc}^{*} and sensed (V_{dc}) dc voltages at n^{th} sampling instant. K_{pd} and K_{id} are proportional and integral gains of dc bus voltagae PI controller.

The reference source current is therefore

$$I_d^{*} = I_{d\,dc} + i_{loss}$$

The reference source current must be in phase with the voltagae at the PCC but non zero sequence componenet. It is therefore obtained by the folling reverce Park's transformation

$$\begin{bmatrix} ia^{*} \\ ib^{*} \\ ic^{*} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix}\begin{bmatrix} id^{*} \\ iq^{*} \\ i0^{*} \end{bmatrix}$$

with I_d^{*} and I_q^{*} and I_0^{*} is as zero.

4 MODELING, RESULT AND DISCUSSION

The performance of single phase SRF theory based control algorithm in time domain for three-phase DSATCOM is simulated using MATLAB with Simulink and simpower system (SPS) toolboxes at distribution level nonlinear loads. The ripple filter is connected to the DsATCOM for filtering the ripple at the PCC voltage. The system data are given in the Appendix.

The control algorithm for DSATCOM is also modelled in MATLAB. The reference source currents are derived from the senced PCC voltages (V_{sa}, V_{sb}, V_{sc}), load currents ($i_{La,}$ i_{Lb}, i_{Lc}) and the dc bus voltage of DSATCOM is V_{dc}. The hysteresis current controller is used over the reference and sensed source currents to generate the gating signals to IGBTs of VSC of DSATCOM. The PCC voltage (V_{abc}), source current (I_{abc}) and load current ($I_{Labc),}$ load voltage (VL_{abc}), terminal voltage ($V_{t)}$ having represented by folling waveforms in fig 4.

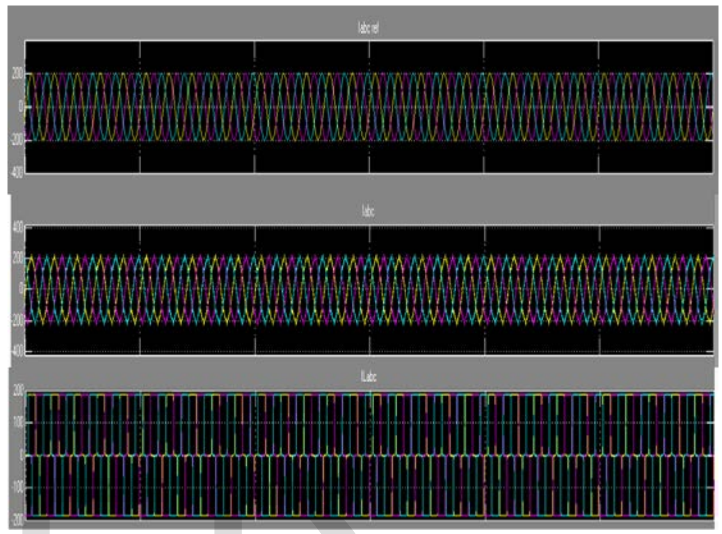

Fig. 4 (a) Performance of Three phase DSTATCOM with SRF theory based control algorithm for PF

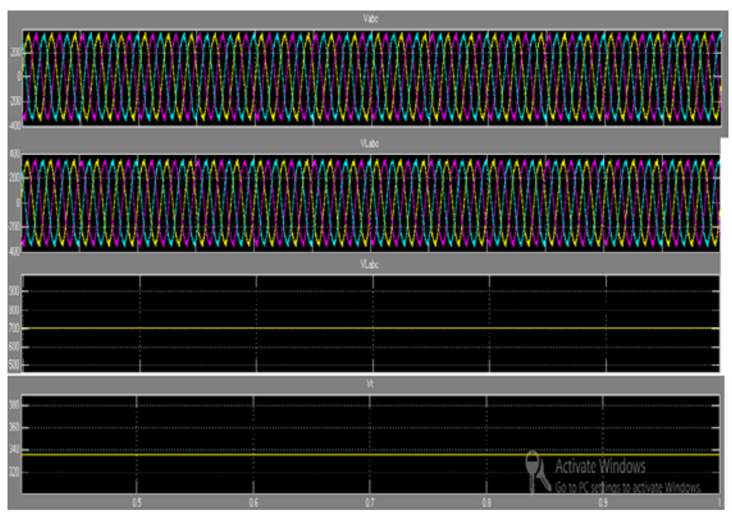

Figure 4(b) Performance of Three phase DSTATCOM with SRF theory based control algorithm for PFC

The totle harmonic distortion (THD) of load current (I_{Labc}) is 27.94% and the THD of source current (I_{Labc}) is 4.34%, that is less than load current THD and at the IEEE standard for better performance THD should be less than 5%. The THD of load and source voltages are same and less than 5% and equal to tha 4.64% as per MATLAB Simulink result, as per norm of

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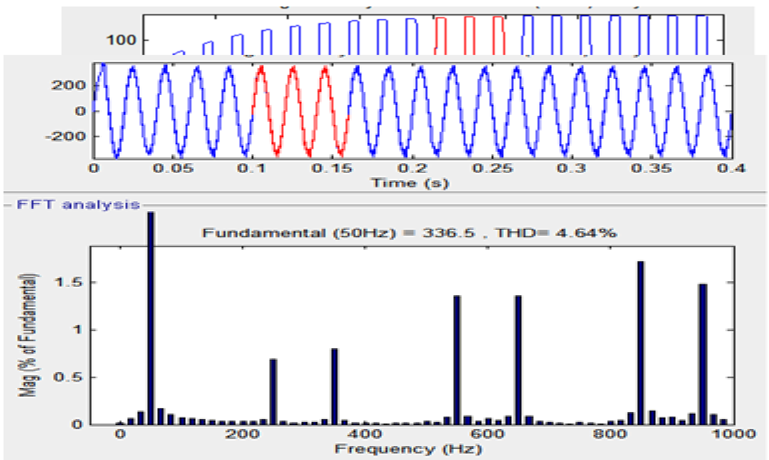
IEEE the THD should be less than 5% id fond. The DC bus voltage (V_{dc}) is constant and equal to the 700 volts. Terminal voltage is also constanat and equal to the reference voltage. Here also found V_{abc} and I_{abc} are also are in same phase and having unity power factor. The THD of V_{abc}, I_{abc} and I_{Labc} are represented in the following fig. 5.

Figure 5 (a) Load current and the harmonic spectrum



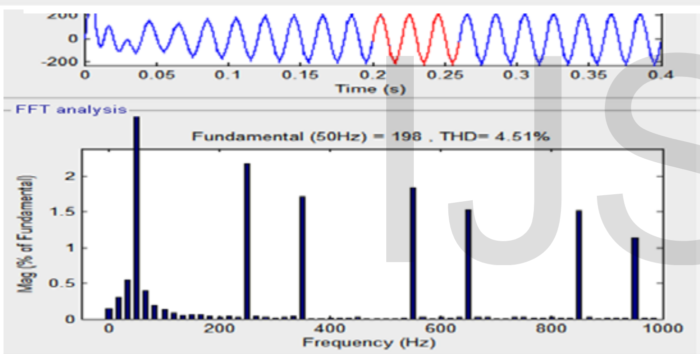


Figure 5 (b) Source current and the harmonic spectrum.

Figure 5 (c) Source/Load Voltage and the harmonic spectrum

5 CONCLUSION

A DSATCOM has been employed for compensation of nonlinear loads at distribution level using synchronous reference frame theory based control algorithm on three phase system. The SRF theory based control algorithm is used for extraction of balanced per phase active and reactive power for generation of reference currents. Various functions of DSATCOM in nonlinear distribution system such as harmonic elimination, source current compensation and load balancing have been demnstrated in power factor correction observed as per expected. The dc bus voltage of the DSATCOM has been regulated to the reference dc bus voltage under all varying loads. Based on simulated and test results, it is concluded that developed DSATCOM and its control algorithm has been found suitable for PFC operation in ttime varyimg loads.

APPENDIX

Ac suuply source: 3-Phase, 415 V (L-L), 50 Hz;
Source Impedance: R_s = .01 Ohm, L_s = .4 mH;
Non Linear Load: Three phase full bridge uncontrolled recti fier with R= 3 ohm and L= 200 mH;
Ripple filter: R_f= 5 ohm and C_f = 10 micro F;
DC bus Capacitance: 3000 micro Farad;
DC bus Voltage: 700 V

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